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## REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

### Status of Claims

Claims 1-17 are pending in the application. Claims 12-17 are withdrawn from consideration. Claims 1-11 have been rejected. Claim 1 has been voluntarily amended.

### CLAIM REJECTIONS

### 35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-5, 7-8, 10 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,807,188 (Casagrande).

In addition, the Examiner rejected claims 1-4, 6-8, 10-11 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,992,980 (Park et al.).

Applicant respectfully traverses the Examiner's rejections, because neither one of the cited references is a sufficient reference for showing anticipation of all the limitations recited in independent claim 1 as filed. However, in the interest of better clarifying the subject matter recited in independent claim 1, Applicant has voluntarily amended independent claim 1. Both cited references clearly fail to teach or suggest the limitations recited in claim 1:

"...**mitigating neighboring effect** by sensing substantially simultaneously a state of adjacent memory cells through **at least a partially shared sensing path**."

Independent claim 1 recites:

1. "A method of reading data in a virtual ground array of memory cells comprising: <u>mitigating neighboring effect</u> by sensing substantially <u>simultaneously</u> a state of adjacent memory cells through <u>at least a partially shared sensing path</u>."

Whereas the Casagrande reference generally teaches:

"An electrically alterable, non volatile memory device capable of enduring a high number of cycles utilizes an array of "semidouble" cells, each formed by a pair of elementary EEPROM cells connected substantially in parallel and a single select transistor. **A special program lines biasing circuit generating a bias voltage representative of a condition wherein one of the two elementary EEPROM structure is broken** and sense amplifiers comprising a comparator circuit comparing the current flowing through an addressed semidouble memory cell with the current flowing through a reference cell comprising a pair of virgin EEPROM type elementary cells **to ensure operability of each bit of the memory also when one of the two elementary cells supporting the bit fails.** Different from known memories, only the EEPROM structure is duplicated while column lines, select lines and ancillary circuitry don't require duplication." (Abstract)

**Casagrande makes no mention of mitigating neighboring effect.**

And the Park reference generally teaches:

"A virtual ground electrically programmable read-only memory device in which disturbance to neighboring cells is practically eliminated, is disclosed. In one embodiment the memory device comprises a plurality of memory cells formed in a semiconductor substrate and arranged in rows and columns so as to form an array. During read operations, pairs of adjacent cells are accessed simultaneously by grounding a single column line within the array. **The two adjacent column lines—one on each side of the grounded column line—are <u>coupled to separate read paths</u>.** Within the array, rows of cells store bits from a plurality of data bytes according to a pattern in which pairs of adjacent cells store different bits from different bytes." (Abstract)

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Although park specifically mentions mitigating neighboring effect, it also explicitly teaches using two separate reading paths. The common column line the Examiner refers to in the prior office action is not part of the sensing or reading path, it is part of the current source path for cells. This fact is known in the art and made clear within the above quoted portion of Park.

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Since the Casagrande reference makes no mention of **mitigating neighboring effect** that may occur during the reading process of a memory array, and the Park reference teaches a device in which "**The two adjacent column lines—one on each side of the grounded column line—are coupled to separate read paths**", neither can be considered an anticipatory reference against pending claim 1.

Claim 1, as clarified is considered allowable in view of the cited prior art. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections of independent claim 1 and all claims dependent from it.

## 35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claim 9 under 35 U.S.C. § 103(a), as being unpatentable over Park in view of U.S. Patent No. 6,975,536 (Maayan et al).

In view of the remarks and arguments above, Applicant asserts that this claim is allowable by virtue of its dependence on an allowable base claim. Reconsideration and withdrawal of the 103 rejection is respectfully requested.
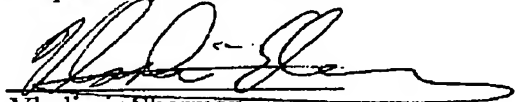
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    In view of the foregoing amendments and remarks, all the pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

    Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

    Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

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